REMARKS

Claims 1-34 were pending in the application. Claim 26 has been cancelled. Claims 1 and 18 have been amended. Claims 1-25 and 27-34 remain pending in the application.

Objection to the Claims:

Claims 1-17 were objected to for an informality in claim 1. Applicant submits that the amended version of claim 1 overcomes this objection.

35 U.S.C. § 112 Rejection:

Claims 18-34 were rejected under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to point out and distinctly claim the subject matter which applicant regards as the invention. Applicant submits the amendment to claim 18 overcomes the rejection.

35 U.S.C. § 103 Rejection:

Claims 1-34 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Knoll, U.S. Patent 6,233,200, in view of Yamazaki, U.S. Patent 6,198,689. Applicant respectfully traverses this rejection.

The cited references, taken singly or in combination, do not teach or suggest all of the elements of the independent claims. Knoll teaches a clock distribution network that includes a phase-locked loop (PLL), clock buffers, an enabling circuit, and a distribution inhibit circuit. The PLL is configured to generate a clock signal and a lock detect signal. The clock buffers are adapted to receive the clock signal from the PLL. The buffers have outputs that can be connected to clock loads. The enabling circuit enables selected buffers to drive the clock loads. The distribution inhibit circuit selectively produces the enable signal to inhibit distribution of the clock signal responsive to the lock detect signal.

Yamazaki teaches an integrated circuit device having a self timing control circuit for generating an input loading timing signal whose phase is adjusted with an external clock, where loading of input signals supplied from outside, such as a command input signal, address input signal and data input signal, to internal circuits is forbidden when the self timing control circuit is adjusting phase. When the self timing control circuit finishes adjusting the phase to a certain degree, the loading operation of an input signal at the input circuit using the input loading timing signal is enabled. To execute such an operation, the input circuit generates an input loading control signal based on a lock-on signal or adjustment signal of the DLL circuit, or based on an input stop cancellation signal, for example. The input circuit controls the stop and restart of loading of the input signal according to this input loading control signal.

In contrast, Applicant's independent claim 1 recites, in pertinent part:

"A source synchronous receiver comprising:
a data buffer configured to receive data through one or more signal lines ...
a digital locked loop (DLL) circuit configured to receive the second clock signal from the clock signal buffer, wherein the DLL circuit is configured to drive the second clock signal to the data buffer" (emphasis added).

Independent claim 18 recites a similar combination of features.

Neither of the cited reference teaches or suggests a data buffer configured to receive data through one or more signal lines, nor does either cited reference teach or suggest a DLL circuit configured to drive a second clock signal to the data buffer. Applicant further submits that, taken in combination, the cited references do not teach or suggest the combination of features as recited in the independent claims.

In the Office Action, the Examiner asserts that Figure 2, elements 2 and 3 of Yamazaki disclose a data buffer using a DLL. Applicant respectfully disagrees with this assertion, and submits that the input buffer 4 that is part of input circuit 3 of Yamazaki

Figure 2 is not a data buffer. Applicant submits that input buffer 4 is coupled to receive only command signals, such as a row address strobe, column address strobe (/RAS and /CAS, respectively, of Yamazaki Figure 2). Applicant notes that these signals are referred to as command signals in column 5, lines 30-31 of Yamazaki. Thus, Applicant submits that Yamazaki does not teach or suggest a data buffer configured to receive data through one or more signal lines as recited in the independent claims.

For at least these reasons, Applicant submits that a case of obviousness has not been established. Accordingly, removal of the 35 U.S.C. § 103(a) rejection is respectfully requested.

CONCLUSION

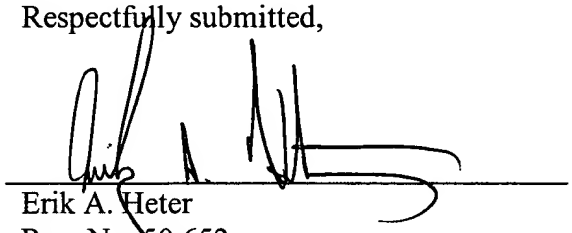
Applicant submits the application is in condition for allowance, and an early notice to that effect is requested.

If any extensions of time (under 37 C.F.R. § 1.136) are necessary to prevent the above referenced application(s) from becoming abandoned, Applicant(s) hereby petition for such extensions. If any fees are due, the Commissioner is authorized to charge said fees to Meyertons, Hood, Kivlin, Kowert, & Goetzel, P.C. Deposit Account No. 501505/5181-76300/BNK.

Also enclosed herewith are the following items:

☒ Return Receipt Postcard

Respectfully submitted,



Erik A. Heter
Reg. No. 50,652
AGENT FOR APPLICANT(S)

Meyertons, Hood, Kivlin, Kowert, & Goetzel, P.C.
P.O. Box 398
Austin, TX 78767-0398
Phone: (512) 853-8800

Date: 10/5/04